

REMARKS

As a preliminary matter, Applicants thank the Examiner for the withdrawal of the previous rejections, and for the acknowledgement of allowable subject matter in claims 12 and 14.

Claims 11 and 13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakami et al. (U.S. 4,380,008) in view of Miyazawa (U.S. 5,731,794). Applicants respectfully traverse this rejection because neither of the cited references, whether taken alone or in combination, discloses or suggests a liquid crystal display device or method having a period during which neither data writing nor data erasing is performed, or more particularly, a device/method where one time frame includes a data writing period, a data erasing period, and a period during which neither writing nor erasing is performed, as in claims 11 and 13 of the present invention.

The Examiner cites Miyazawa only for teaching an active matrix type display device, and not for being analogous to any of the other features or limitations of the present invention. The Examiner relies only upon the teaching of Kawakami as support for the timing period features of the present invention. The portions of Kawakami that are cited by the Examiner, however, fail to teach or suggest the timing features of in the present invention relating to the period where neither data writing nor erasing is performed (“the non-operation period”) or the one time frame that includes all of a writing period, an erasing period, and a non-operation period.

Specifically, the Examiner asserts, on page 3 of the outstanding Office Action (Paper No. 8), that the selected state and half-selected state (Fig. 9) are analogous to the “data writing processing,” that the erasing state (also Fig. 9) is analogous to the “data erasing process,” and that the non-selected state (Fig. 9) is somehow analogous to the non-operation period of the present invention. These assertions are erroneous, however, for several reasons.

First, claims 11 and 13 do not recite “data writing processing” and “data erasing process” method steps, as asserted by the Examiner. Instead, independent claims 11 and 13 actually recite a period of the data writing process, and a period of the data erasing process. These distinctions are not insignificant, because the recited claim terms refer to a timing for such processes, while the Examiner appears to refer to the overall process steps themselves, and not to their respective timings.

Second, the “non-selected state” is not analogous to the non-operation period of the present invention. As clearly shown in Fig. 9 of Kawakami, a voltage of $\pm 1/a^*V_0$ is always applied to the non-selected state. Because this voltage is constantly applied, it cannot be analogous to the non-operation period of the present invention where neither data writing nor data erasing is performed. The present invention is therefore clearly distinct from Kawakami in at least these respects.

In fact, Kawakami is very much different from the present invention because the several “states” from Kawakami do not even refer to timings. Kawakami defines, at col. 4, lines 1-10, the meanings of the term “selected state,” “half-selected state,” and the “non-

selected state.” Kawakami expressly teaches that the respective “states” do not refer to the timing of individual processes, but instead the *crossing points* of voltages applied to perpendicular crossing linear electrodes. According to Kawakami, the “non-selected state” does not refer to a non-operation timing period at all, but instead only to a physical *crossing point* of two linear electrodes having no applied voltage. Accordingly, the Examiner has not identified features from Kawakami that are analogous to the present invention. The *prima facie* case of obviousness is therefore deficient.

Section 2143.03 of the MPEP requires of the Examiner, when attempting to establish a *prima facie* case of obviousness against a claimed invention, to first cite to where in the prior art is taught or suggested each and every feature and limitation of the claimed invention. In the present case, however, the Examiner has not done so. As discussed above, the crossing points of perpendicular electrodes taught by Kawakami have nothing to do with the specific timing features of the present invention.

Applicants submit that the Kawakami reference, and the Miyazawa reference as well, both fail to teach or suggest a timing for a liquid crystal display device where one frame period includes a period for data writing, a period for data erasing, and a period during which neither data writing nor data erasing is performed. Because the Examiner has not cited to any such features in either of the prior art references, the Section 103 rejection of claims 11 and 13 based on a combination of Kawakami and Miyazawa is respectfully traversed, and should be withdrawn.

Moreover, Kawakami is further different from the present invention because the reference teaches to apply a holding voltage V_{NS} all through the “period in which the holding voltage is applied.” (Col. 4, line 54, to col. 5, line 10). Because the phase transition liquid crystal changes its state in accordance with Kawakami’s mean value of voltage, Kawakami is required to constantly be writing one of its holding voltage V_{NS} , write-in voltage VS , and erasing voltage VE to maintain the state of the liquid crystal. When this system is applied to a TFT panel, it is impossible for Kawakami to use an amplitude selection method as its driving method of phase transition liquid crystal because the pixel charge in a TFT would be held until a next writing operation. Such a method is very different from an amplitude selection method, and therefore the present invention.

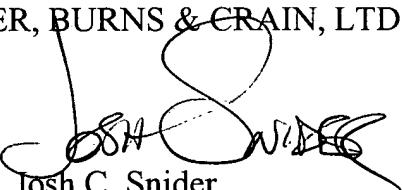
In contrast, the present invention is able to completely stop scanning a TFT panel during the claimed non-operation period, and thus overcome the limitations of Kawakami discussed above. Such clear advantages over the prior art are to be taken into consideration by the Examiner, in addition to other prior art deficiencies, in determining the appropriateness of attempting to establish and/or maintain a rejection based on obviousness. These clear advantages of the present invention over the prior art further demonstrate why the outstanding obviousness rejection should be withdrawn.

For all of the foregoing reasons, Applicants submit that this Application, including claims 11-14, is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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